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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/848,778	05/03/2001	Peter A. Beerel	06666-077001/USC3027	6633
20985	7590	06/19/2007	EXAMINER	
FISH & RICHARDSON, PC P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022				TORRES, JOSEPH D
ART UNIT		PAPER NUMBER		
		2112		
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Advisory Action</b> <b>After the Filing of an Appeal Brief</b>	Application No.	Applicant(s)
	09/848,778	BEEREL ET AL.
	Examiner Joseph D. Torres	Art Unit 2112

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

The reply filed 09 April 2007 is acknowledged.

1.  The reply filed on or after the date of filing of an appeal brief, but prior to a final decision by the Board of Patent Appeals and Interferences, will not be entered because:

a.  The amendment is not limited to canceling claims (where the cancellation does not affect the scope of any other pending claims) or rewriting dependent claims into independent form (no limitation of a dependent claim can be excluded in rewriting that claim). See 37 CFR 41.33(b) and (c).

b.  The affidavit or other evidence is not timely filed before the filing of an appeal brief. See 37 CFR 41.33(d)(2).

2.  The reply is not entered because it was not filed within the two month time period set forth in 37 CFR 41.39(b), 41.50(a)(2), or 41.50(b) (whichever is appropriate). Extensions of time under 37 CFR 1.136(a) are not available.

Note: This paragraph is for a reply filed in response to one of the following: (a) an examiner's answer that includes a new ground of rejection (37 CFR 41.39(a)(2)); (b) a supplemental examiner's answer written in response to a remand by the Board of Patent Appeals and Interferences for further consideration of rejection (37 CFR 41.50(a)(2)); or (c) a Board of Patent Appeals and Interferences decision that includes a new ground of rejection (37 CFR 41.50(b)).

3.  The reply is entered. An explanation of the status of the claims after entry is below or attached.

4.  Other: See attached remarks

JOSEPH D. TORRES  
PRIMARY EXAMINER  
TECHNOLOGY CENTER 2100

**Response to Reply Brief**

On page 1, paragraph 3 of the Appellant's Reply brief, the Appellant contends, "On page 16, the rejection points out that "prefix and suffix operations" have been developed independently in error correction and computational mathematics/computer science". This statement does not appear to be supported by any evidence in the case, and with all due respect is improper for that reason".

The Examiner asserts that the statement is made based on extensive search. As pointed out in the previous Examiner's answer, if the word "parallel" were removed from in front of the phrase "prefix and suffix operations" in claim 1, then Viterbi would teach each and every element of claim 1 (see rejection of claim 1, above), which the Appellant does not dispute and in fact agrees with (Appellant's response, page 3, 04/12/2006).

If a Prior Art existed that jointly covered Parallel Prefix and Suffix operations with the intended use in a SISO decoder, then such a Prior Art could be used in a 35 USC § 102 rejection of claim 1. The Examiner reminds the Appellant of an Applicant's duty to disclose under 37 CFR § 1.56. If the Applicant is asserting that such an art exists, such an assertion provides further evidence that the Examiner's rejection should be maintained.

On page 2, last paragraph of the Appellant's Reply brief, the Appellant contends, "This compares with the present situation, where the secondary reference does not say anything about teaching to speed up computation, but rather teaches the opposite".

The last paragraph on page 7 to first paragraph on page 8 of Leighton explicitly teaches that it is desirable to develop parallel algorithms with as much a speed-up as possible. This concept explicitly taught in Leighton is fundamental to parallel processing that any faculty in Computer Science, Computational Mathematics or Engineering should know and take for granted and has been fundamental for decades (see col. 1, lines 19-24 in US 4247892 A and col. 1, lines 21-31 in US 4101960 A).

On page 2, last paragraph of the Appellant's Reply brief, the Appellant contends that "Thomson Leighton reference has data dependencies that prevent it from being parallelized", which make absolutely no sense since referring to the last paragraph on page 7 to first paragraph on page 8 of Leighton, the Leighton reference is about parallelizing serial algorithms.

On page 3, first paragraph of the Appellant's Reply brief, the Appellant contends, "The issue here is whether the serial operations in Thomson Leighton could be parallelized", which makes absolutely no sense since Leighton is about converting serial algorithms to parallel algorithms and not a discussion on serial algorithms.

On page 3, second paragraph of the Appellant's Reply brief, the Appellant contends, "At the bottom of page 21, a very troubling statement is made. The patent office appears to indicate that whether the Board reverses this case or not, that the "examiner will determine the best way to proceed"".

That is correct.

On page 3, second paragraph of the Appellant's Reply brief, the Appellant contends, "It is believed to be wholly improper for the Examiner to make statements suggesting that he will make another rejection if the Board reverses this one".

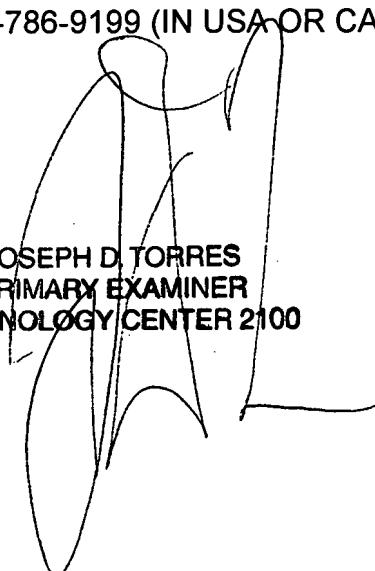
In view of the overwhelming evidence, the Examiner does not believe that the Examiner will be reversed. However, if the Examiner is reversed, based on the overwhelming evidence in the art, the Examiner can only conclude that a reversal would be due to errors in the Examiner's rejection and not the deficiencies in the art. The Examiner is requesting feedback from the board in the case that the Examiner is reversed.

Even if the Examiner is reversed, the Examiner is still responsible for determining the allowability of a case.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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